287529US0X PCT

MAR 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:

Yoshiyuki FUKUDA, et al.

SERIAL NO: Nev

New U.S. PCT Application Based on PCT/JP04/14528

GAU:

FILED:

Herewith

EXAMINER:

FOR:

CERAMIC CIRCUIT BOARD, METHOD FOR MAKING THE SAME, AND POWER MODULE

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

The applicant(s) wish to make of record the references listed on the attached form P10-1449. Copies of the listed
references are attached, where required, as are either statements of relevancy or any readily available English
translations of pertinent portions of any non-English language references.
A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

	Attached is a list of applicant's pending application(s), published application(s) or issued patent(s) which may be related to the present application. In accordance with the waiver of 37 CFR 1.98 dated September 21, 2004, copies of the cited pending applications are not provided. Cited published and/or issued patents, if any, are listed on the attached PTO form 1449.						
	A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).						
THE PERSON NAMED IN COLUMN TO THE PE							

CERTIFICATION

Each item of information contained in this information disclosure statement was first cited in any communication	nication
from a foreign patent office in a counterpart foreign application not more than three months prior to the fi	ling of
this statement.	

□ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number <u>15-0030</u>. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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Form PTO 1449 U.S. DEPARTMENT OF COMMERCE (Modified) PATENT AND TRADEMARK OFFICE			ATTY DOCKET NO. 287529USOX PCT APPLICANT Yoshiyuki FUKUDA, et al. FILING DATE Herewith		SERIAL NO. New U.S. PCT Application Based on PCT/JP04/14528 , GROUP			
LIST OF REFERENCES CITED BY APPLICANT								
			•	U.S. PATENT DOCUMENTS				
EXAMINER		DOCUMENT			01.400	SUB	FILING DATE	
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	AO	5-166968	07/02/93	JP			NO	
	AP	2001-144234	05/25/01	JP			NO	
	AQ	2002-111211	04/12/02	JP			NO	
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New U.S. PCT Application Based on PCT/JP04/14528 Yoshiyuki FUKUDA, et al. Docket No. 287529 US

STATEMENT OF RELEVANCY

- 1) References AO AQ have been cited in the International Search Report. A copy of these references is being submitted herewith.
- 2) References have been cited in the corresponding copy of these references is being submitted herewith.
- 3) References are discussed in the specification. A copy of these references is being submitted herewith.
- 4) Reference AA is additional prior art known to Applicant. A copy of this reference is being submitted herewith.
- AA "Ceramic Circuit Board", Takayuki Naba et al., United States Patent No. 6 426 154 B1. Filing Date September 25, 2000. Date of Patent July 30, 2002.

This prior art information discloses a ceramic circuit board comprising: a ceramic substrate and a metal circuit plate bonded to the ceramic substrate through a brazing material layer; wherein the brazing material layer is composed of AI-Si group brazing material and an amount of Si contained in the brazing material is 7 wt% or less. In addition, it is preferable to form a thinned portion, holes, or grooves to outer peripheral portion of the metal circuit plate. According to the above structure of the present invention, there can be provided a ceramic circuit board having both high bonding strength and high heat-cycle resistance, and capable of increasing an operating reliability as electronic device.